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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,708	12/11/2003	Mark R. Visokay	TI-35227	2373

23494 7590 10/20/2005

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EXAMINER	
PHAM, THANHHA S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,708	VISOKAY ET AL.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) *14-21,28-32,58-62 and 67* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,22-27,33-57 and 63-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/11/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Applicant's Election dated 07/28/2005.

Election/Restrictions

1. Applicant's election of claims 1-13, 22-27, 33-57 and 63-66 in the reply filed on 07/28/2005 read on species A-1/B-1 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims 14-21, 28-32 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected species.

Oath/Declaration

3. Oath/Declaration filed on 12/11/2003 has been considered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-13, 22-27, 33-57 and 63-66 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

► With respect to claim 1,

lines 3-4, 6 and 8, it is not clear that "a gate electrode" in each of claimed steps are the same or different.

lines 5 and 7, "the deposited high-k dielectric" lacking antecedent basis should be changed to "the deposited high-k gate dielectric layer" to clarify scope of claim.

In addition, it is not clear the claimed step of lines 5-6 (a first anneal) refers to which step of embodiment of figure 2 – step 62 or step 82? it is not clear the claimed step of lines 7-8 (a second anneal) refers to which step of embodiment of figure 2 – step 64 or step 84? <see contraction between claims 2 and 33 for details>

► With respect to claims 26 and 33

"the high-k dielectric layer" lacking antecedent basis should be changed to "the deposited high-k gate dielectric layer.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2, 22-26, 65 and 66, as being best understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Colombo et al [US 6,809,370].

► With respect to claims 1-2, 22-26 and 65, Colombo et al (figs 1-4, col 1-7) discloses the claimed method for treating a deposited high-k dielectric layer during fabrication of a semiconductor device comprising:

nitriding a deposited high-k gate dielectric layer (110, figs 1 & 2B, col 6 lines 7-40) prior to forming a gate electrode (120), wherein nitriding the deposited high-k gate dielectric layer comprises performing a plasma nitridation process;

performing a first anneal of the deposited high-k gate dielectric layer (110) in a non-oxidizing ambient prior to forming said gate electrode (120, figs 1 & 2B, col 7 lines 7-15); and

performing a second anneal of the deposited high-k gate dielectric layer (110) in an oxidizing ambient prior to forming said gate electrode (120, fig 1 & 2B, col 7 lines 15-25) wherein the second annealing is performed at a temperature of about 700 degree C or less (e.g. 400) and atmospheric pressure of about 1 torr or less (e.g. 1 torr),

wherein the second anneal is performed after nitriding the high-k dielectric layer and after performing the first anneal.

► With respect to claim 66, Colombo et al (figs 1-4, col 1-7) discloses the claimed method of fabricating a transistor gate structure, the method comprising:

depositing a high-k gate dielectric layer (110, figs 1 & 2B) above a semiconductor body (104);

nitriding the deposited high-k gate dielectric layer (110, figs 1 & 2B, col 6 lines 7-40);

performing a first anneal of the deposited high-k dielectric gate dielectric layer (110) in a non-oxidizing ambient (120, figs 1 & 2B, col 7 lines 7-15); and

performing a second anneal of the deposited high-k gate dielectric layer (110) in an oxidizing ambient (120, fig 1 & 2B, col 7 lines 15-25);

forming a gate electrode material layer (120, fig 1 & 2C) above the deposited high-k gate dielectric layer after nitriding and after performing the first and second anneals; and

patterning the gate electrode material layer and the deposited high-k gate dielectric layer to form a patterned gate structure (figs 2D and 1).

6. Claims 1, 63-65 and 66, as being best understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Jung et al [US 6,875,678].

► With respect to claim 1, 63 and 65, Jung et al (figs 1-11B, cols 1-10) discloses the claimed method for treating a deposited high-k dielectric layer during fabrication of a semiconductor device comprising:

nitriding a deposited high-k gate dielectric layer (12, col 5 lines 8-67, col 7 lines 58-67) prior to forming a gate electrode (14), wherein nitriding the deposited high-k gate dielectric layer comprises performing a nitridation anneal in nitrogen containing ambient wherein the nitridation anneal is performed at a temperature of about 1000 degrees C or less and wherein the nitrogen containing ambient comprises NH_3, OR nitriding the

deposited high-k gate dielectric layer comprises performing a plasma nitridation process;

performing a first anneal of the deposited high-k dielectric (12) in a non-oxidizing ambient prior to forming said gate electrode (col. 8 lines 1-7); and

performing a second anneal of the deposited high-k dielectric (12) in an oxidizing ambient prior to forming said gate electrode (col 7 lines 64-67 and col 8 lines 1).

► With respect to claim 66, Jung et al (figs 1-11B, cols 1-10) discloses the claimed method of fabricating a transistor gate structure, the method comprising:

depositing a high-k gate dielectric layer (12, fig 1) above a semiconductor body (10);

nitriding the deposited high-k gate dielectric layer (12, col 5 lines 8-67, col 7 lines 58-67);

performing a first anneal of the deposited high-k dielectric gate dielectric layer (12) in a non-oxidizing ambient (col 8 lines 1-7); and

performing a second anneal of the deposited high-k gate dielectric layer (12) in an oxidizing ambient (col 7 lines 64-67 and col 8 lines 1);

forming a gate electrode material layer (14, col 8 lines 8-14) above the deposited high-k gate dielectric layer after nitriding and after performing the first and second anneals; and

patterning the gate electrode material layer and the deposited high-k gate dielectric layer to form a patterned gate structure (fig 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1 and 33-51, as being best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Jung et al [US 6,875,678] in view of Vosokay et al [US 2003/0129817].

► With respect to claims 1, 33, 39-42, 44, 47-51, Jung et al (figs 1-11B, cols 1-10) discloses a method for treating a deposited high-k dielectric layer during fabrication of a semiconductor device comprising:

nitriding a deposited high-k gate dielectric layer (12, col 5 lines 8-67, col 7 lines 58-67) prior to forming a gate electrode (14), wherein nitriding the deposited high-k gate dielectric layer comprises performing a nitridation anneal in nitrogen containing ambient wherein the nitridation anneal is performed at a temperature of about 1000 degrees C or less and wherein the nitrogen containing ambient comprises NH_3, OR nitriding the deposited high-k gate dielectric layer comprises performing a plasma nitridation process; and

performing a third anneal of the deposited high-k dielectric (12) in a non-oxidizing ambient after nitriding the deposited high-k gate dieledtric layer wherein the non-oxidizing ambient comprises N2, Ar, He or Ne (col. 8 lines 1-7).

Jung et al does not teach performing first and second anneals prior to nitriding the deposited high-k gate dielectric layer and prior to forming a gate electrode wherein said first anneal being performed in a non-oxidizing ambient comprised N2, Ar, or He and said second anneal being performed in an oxidizing ambient, said first anneal being performed prior to said second anneal.

However, Visokay et al teaching first anneal the high-k gate dielectric layer in the non-oxidizing ambient prior nitridizing the high-k gate dielectric layer (text [0010]-[0011]: first annealing the high-k gate dielectric layer of MO or MsiO) and second anneal high-k gate dielectric layer in the non-oxidizing ambient prior nitridizing the high-k gate dielectric layer (text [0010], [0012]-[0013]: second annealing the high-k gate dielectric layer of MO or MsiO) to densify and to heal defects the high-k gate dielectric layer (104).

Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Jung et al by performing the first and second anneals as being claimed to improve characteristic of the high-k gate dielectric layer as being mentioned above.

► With respect to claims 34-38, 43, 45-46, the claimed ranges of parameters for first, second and third anneals are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller 105 USPQ233, 255 (CCPA 1955)., the selection of reaction parameters such as temperature and concentration would have been obvious.

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

8. Claims 1, 33-57, as being best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Colombo et al [US 6,809,370] in view of Visokay et al [US 2003/0129817].

Colombo et al al (figs 1-4, col 1-7) discloses a method for treating a deposited high-k dielectric layer during fabrication of a semiconductor device comprising:

nitriding a deposited high-k gate dielectric layer (110, figs 1 & 2B, col 6 lines 7-40) prior to forming a gate electrode (120), wherein nitriding the deposited high-k gate dielectric layer comprises performing a plasma nitridation process;

performing a third anneal of the deposited high-k gate dielectric layer (110) in a non-oxidizing ambient comprised N2, Ar, He or Ne after nitriding the deposited high-k gate dielectric (figs 1 & 2B, col 7 lines 7-15); and

performing a fourth anneal of the deposited high-k gate dielectric layer (110) in an oxidizing ambient after performing the third anneal.

Colombo et al does not teach performing first and second anneals prior to nitriding the deposited high-k gate dielectric layer and prior to forming a gate electrode wherein said first anneal being performed in a non-oxidizing ambient comprised N2, Ar, or He and said second anneal being performed in an oxidizing ambient, said first anneal being performed prior to said second anneal.

However, Visokay et al teaching first anneal the high-k gate dielectric layer in the non-oxidizing ambient prior nitridizing the high-k gate dielectric layer (text [0010]-[0011]: first annealing the high-k gate dielectric layer of MO or MsiO) and second anneal high-k gate dielectric layer in the non-oxidizing ambient prior nitridizing the high-k gate dielectric layer (text [0010], [0012]-[0013]: second annealing the high-k gate dielectric layer of MO or MsiO) to densify and to heal defects the high-k gate dielectric layer (104).

Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Colombo et al by performing the first and second anneals as being claimed to improve characteristic of the high-k gate dielectric layer as being mentioned above.

With respect to the claimed ranges parameters of the first, second, third and fourth anneals, the claimed range parameters are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. See *In re Aller 105 USPQ233, 255 (CCPA 1955); In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

9. Claims 1-13, as being best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Jung et al [US 6,875,678] in view of Harada [US 6,642,131].

Jung et al (figs 1-11's, col 1-10) discloses a method for treating a depositing high-k gate dielectric layer during fabricating a semiconductor device comprising:

nitriding a deposited high-k gate dielectric layer (12, col 5 lines 8-67, col 7 lines 58-67) prior to forming a gate electrode (14), wherein nitriding the deposited high-k gate dielectric layer comprises performing a nitridation anneal in nitrogen containing ambient wherein the nitridation anneal is performed at a temperature of about 1000 degrees C or less and wherein the nitrogen containing ambient comprises NH_3, OR nitriding the deposited high-k gate dielectric layer comprises performing a plasma nitridation process; and

performing a second anneal of the deposited high-k dielectric (12) in an oxidizing ambient prior to forming said gate electrode (col 7 lines 64-67 and col 8 lines 1).

Jung et al does not teach performing a first anneal of the deposited high-k gate dielectric layer in a non-oxidizing ambient prior to nitriding the deposited high-k gate dielectric layer.

However, Harada (figs 7B-7C, col 14) discloses performing the first anneal of the deposited high-k gate dielectric layer (22A) in the non-oxidizing ambient prior to nitriding the deposited high-k gate dielectric layer to improve thermal stability of the high-k gate dielectric layer.

Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Jung et al by performing the first anneal as being claimed as taught by Harada to improve the thermal stability of the high-k gate dielectric layer.

With respect to the claimed ranges parameters of the first and second anneals, the claimed range parameters are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. See *In re Aller 105 USPQ233, 255 (CCPA 1955); In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

10. Claims 26-27 and 56-57, as being best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Colombo et al [US 6,809,370] or Colombo et al [US 6,809,370] in view of Visokay et al [US 2003/0129817] as applied to claims 22 and 52 above, and further in view of Visokay et al [US 2003/0045080].

Colombo et al or Colombo et al in view of Visokay et al ('817) substantially discloses the claimed method but is silent about using the oxidizing ambient of oxidizing liquid solution comprises $H_2O + H_2O_2$ to expose the deposited high-k gate dielectric layer.

However, Visokay et al ('080) discloses exposing the deposited high-k gate dielectric layer to the oxidizing liquid solution comprises $H_2O + H_2O_2$ to avoid degradation of the overall dielectric constant of the deposited high-k gate dielectric layer.

Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Colombo et al or Colombo et al in view of Visokay et al ('817) by exposing the high-k gate dielectric layer to the oxidizing liquid solution as being claimed, per taught by Visokay et al ('080), to avoid degradation of the overall dielectric constant of the deposited high-k gate dielectric layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thanhha Pham
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